3. Recommended Operating Conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	PV_{CC}, AV_{CC}	5		26	V
V_{IH}	High-level input voltage	AM0, AM1, AM2, MUTE, SDZ, SYNC, MODSEL	2			V
V_{IL}	Low-level input voltage	AM0, AM1, AM2, MUTE, SDZ, SYNC, MODSEL			0.8	V
V_{OL}	Low-level output voltage	FAULTZ, $R_{PULL-UP}$ = 100 k , PV_{CC} = 26 V			0.8	V
I_{IH}	High-level input current	AM0, AM1, AM2,				



6. AC Electrical Characteristics

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
KSVR	Power supply ripple rejection	200 mV_{PP} ripple at 1 kHz, Gain = 26 dB, Inputs AC-coupled to GND		70		dB
P_O	Continuous output power	THD+N = 10%, f = 1 kHz, PV_{CC} = 14.4 V		25		W
		THD+N = 10%, f = 1 kHz, PV_{CC} = 21 V		50		
		THD+N = 10%, f = 1 kHz, PV_{CC} = 24 V		70		
THD+N	Total harmonic distortion + noise	V_{CC} = 21 V, f = 1 kHz, P_O = 15 W (half-power)		0.1%		
Vn	Output integrated noise	20 Hz to 22 kHz, A-weighted filter, Gain = 20 dB		100		µV
				78		dBV
	Crosstalk					

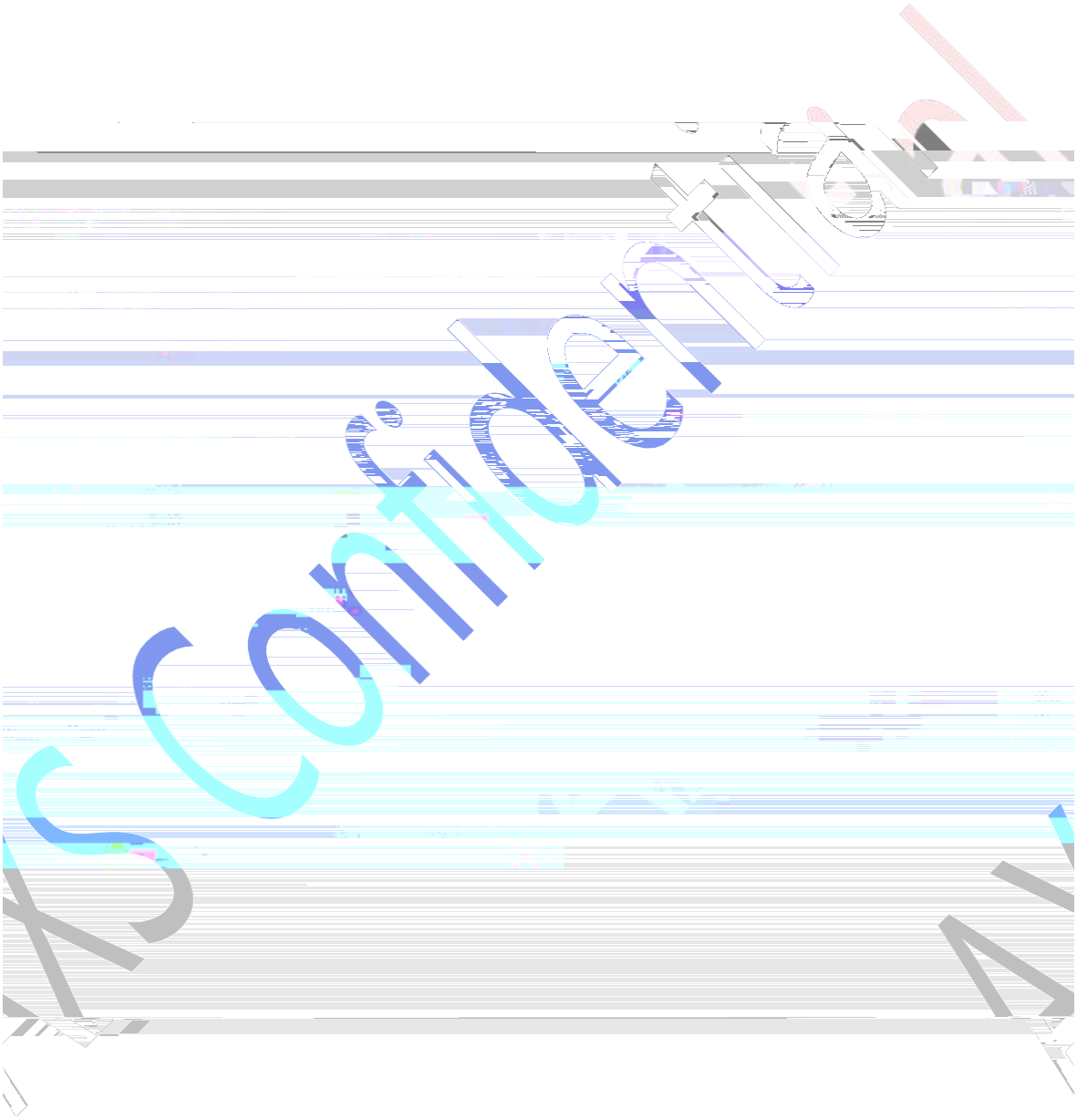
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7. Typical Characteristics



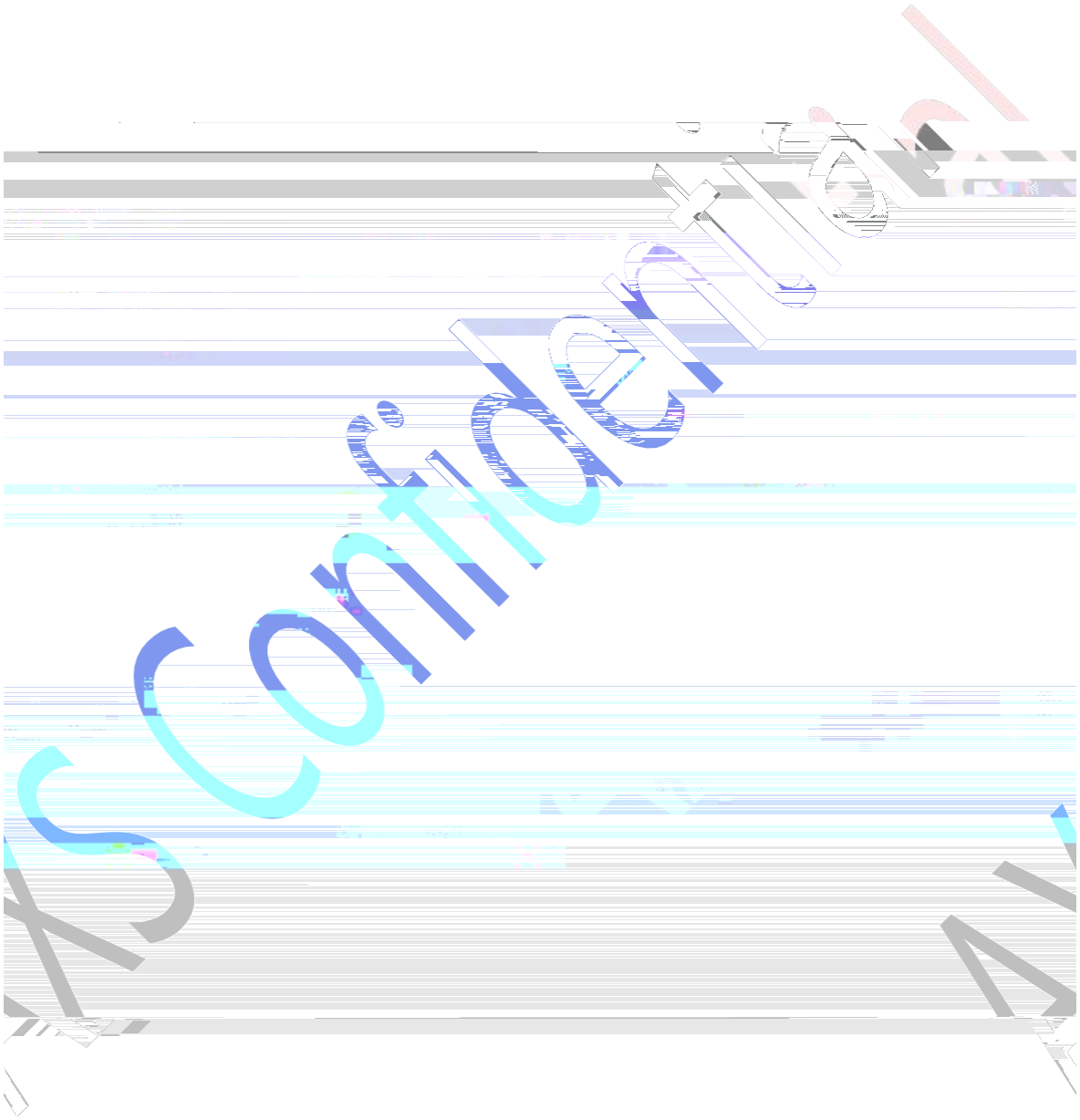
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Typical Characteristics (continued)



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Typical Characteristics (continued)



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3. Feature Description

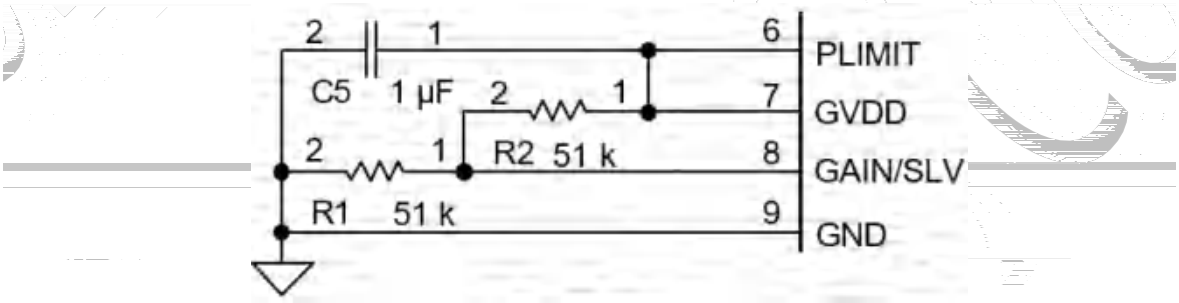
3.1 Gain Setting and Master and Slave

The gain of the AXS2050 is set by the voltage divider connected to the GAIN/SLV control pin. Master or Slave mode is also controlled by the same pin. An internal ADC is used to detect the 8 input states. The first four states set the GAIN in Master mode with gains of 20, 26, 32, and 36 dB respectively, while the next four states set the GAIN in Slave mode with gains of 20, 26, 32, and 36 dB respectively. The gain setting is latched during power- up and cannot be changed while the device is powered on.

1 lists the recommended resistor values for different state settings.

1. Gain and Master/Slave

MASTER / SLAVE MODE	GAIN	R1 (to GND)(1)	R2 (to GVDD)(1)	INPUT IMPEDANCE
Master	20 dB	5.6 k	OPEN	60 k
Master	26 dB	20 k	100 k	30 k
Master	32 dB	39 k	100 k	15 k
Master	36 dB	47 k	75 k	9 k
Slave	20 dB	51 k	51 k	60 k
Slave	26 dB	75 k	47 k	30 k
Slave	32 dB	100 k	39 k	15 k
Slave	36 dB	100 k	16 k	9 k



25. Gain, Master/Slave

In Master mode, the SYNC terminal is an output, while in Slave mode, the SYNC terminal is an input for a clock. TTL logic levels with compliance to GVDD.

3.2 Input Impedance

The AXS2050 input stage is a fully differential input stage and the input impedance changes with the gain 1 lists the values from min to max gain. The tolerance

inputs must be AC-coupled to minimize the output DC-offset and ensure correct ramping of the output voltages during power-ON and power-OFF.

27. Power Limit Example

The PLIMIT circuit sets a limit on the output peak-to-peak voltage. This is done by limiting the duty cycle to a fixed maximum value. The limit can be considered as a "virtual" voltage rail which is lower than the supply connected to PVCC. The "virtual" rail is

$$P_{OUT} = \frac{\left(\left(\frac{R_L}{R_L + 2 \times R_S}\right) \times V_P\right)^2}{2 \times R_L} \quad \text{for unclipped power}$$

3.6 BSPx and BSNx Capacitors

The full H-bridge output stages use only NMOS transistors. Therefore, they require bootstrap capacitors for the high side of each output to turn on correctly. A 220-nF ceramic capacitor of quality X5R or better, rated for at least 16 V, must be connected from each output to the corresponding bootstrap input. (See the application circuit diagram in 32.) The bootstrap capacitors connected between the BSxx pins and corresponding output function as a floating power supply for the high-side N-channel power MOSFET gate drive circuitry. During each high-side switching cycle, the bootstrap capacitors hold the gate-to-source voltage high enough to keep the high-side MOSFETs turned on.

3.7 Differential Inputs

The differential input stage of the amplifier cancels any noise that appears on both input lines of the channel. To use the AXS2050 with a differential source, connect the positive lead of the audio source to the RINP or LINP input and the negative lead from the audio source to the RINN or LINN input.

To use the AXS2050 with a single-ended source, AC ground the negative input through a capacitor equal in value to the input capacitor on positive and apply the audio source to either input. In a single-ended input application, the unused input should be AC grounded at the audio source instead of at the device input for best noise performance. For good transient performance, the impedance seen at each of the two differential inputs should be the same.

The impedance seen at the inputs should be limited to an RC time constant of 1 ms or less if possible to allow the input

be

3.9 DC Detect Protection

The AXS2050 has circuitry which protects the speakers from DC current which might occur due to defective capacitors on the input or shorts on the printed circuit board at the inputs. A DC detect fault is reported on the FAULT pin as a low state. The DC Detect fault causes the amplifier to shutdown by changing the state of the outputs to Hi



4. Device Modulation Scheme

The AXS2050 is internally fixed to BD mode for better performance.

This is a modulation scheme that allows operation without the classic LC reconstruction filter when the amp is driving an inductive load with short speaker wires.

Each output is switching from 0 volts to the supply voltage. The OUTPx and OUTNx are in phase with each other with no input so that there is little or no current in the speaker.

The duty cycle of OUTPx is greater than 50% and OUTNx is less than 50% for positive output voltages. The duty cycle of OUTPx is less than 50% and OUTNx is greater than 50% for negative output voltages.

The voltage across the load sits at 0V throughout most of the switching period, reducing the



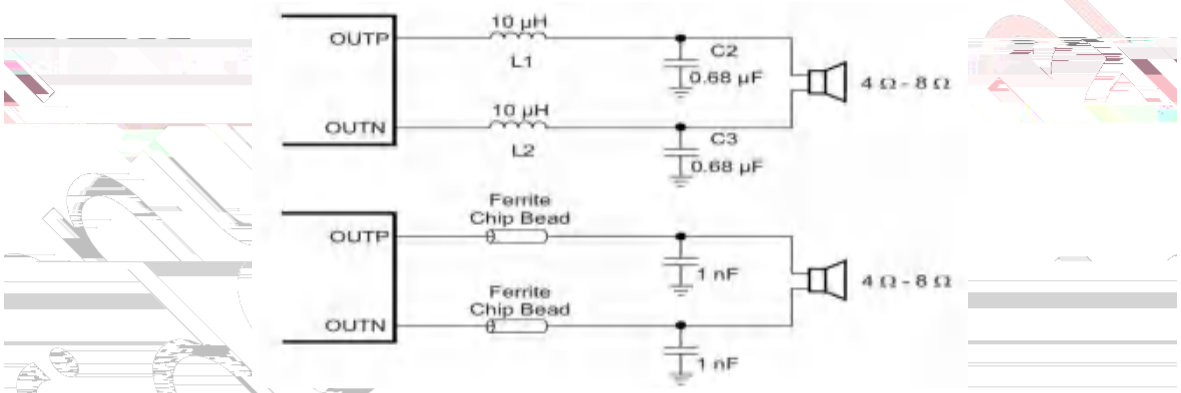
The modulation schemes implemented in the AXS2050 have little loss in the load even without a filter because the pulses are short and the change in voltage is VCC instead of 2 × VCC. As the output power increases and the pulses widen, the ripple current can go up. In this case, the ripple current can be filtered with an LC filter for increasand



7. When to Use an Output Filter for EMI Suppression

A complete LC reconstruction filter should be added in some circuit instances. These circumstances might occur if there are nearby circuits which are sensitive to noise. In these cases, a classic second order Butterworth filter similar to those shown in 29 can be used.

Some systems have little power supply decoupling from the AC line but are also subject to line conducted interference (LCI) regulations. These include systems powered by "wall warts" and "power bricks." In these cases, LC reconstruction filters can be the lowest-cost methods to pass LCI tests. Common mode chokes using low frequency ferrite material can also be effective in preventing line conducted interference.



29. Output Filters

8. AM Avoidance EMI Reduction

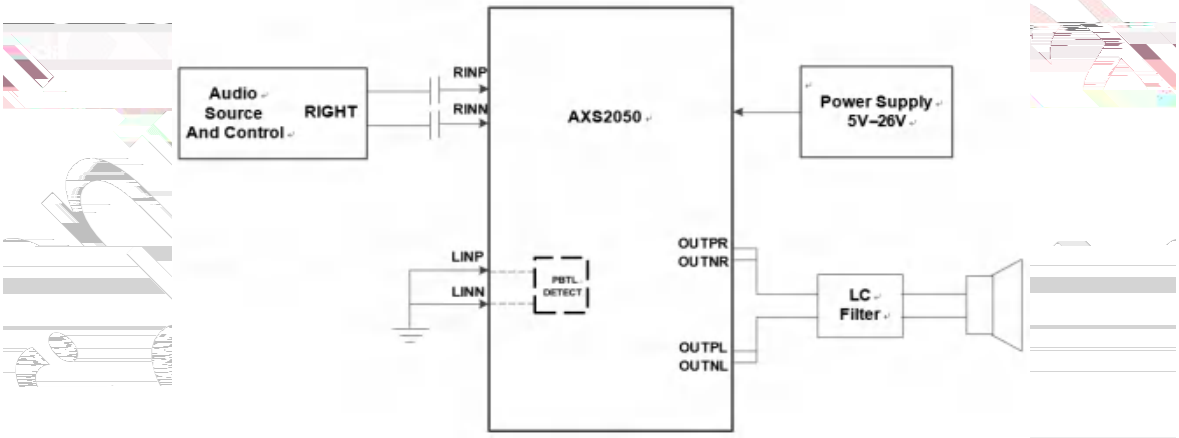
9.1 Mono PBTL Mode

In mono PBTL mode, the device can deliver up to 100-W output power. Configuration steps for mono PBTL mode are as follows:

Connect LINP and LINN directly to Ground (without capacitors), so the device is set in a mono PBTL mode during power up.

Connect OUTPR and OUTNR together for the positive speaker terminal, and OUTNL and OUTPL together for the negative speaker terminal.

- Analog input signal is applied to RINP and RINN.



30. Mono PBTL Mode

9.2 Mono BTL Mode (Single Channel Mode)

The AXS2050 can be connected in mono BTL mode while cutting the idle power-loss nearly by half.

- Connect RINP and RINN directly to Ground (without capacitors), so the device is set in mono BTL mode during power up.
- Connect OUTPL to the positive speaker terminal, and OUTNL to the negative speaker terminal.
- Analog input signal is applied to LINP and LINN.

31. Mono BTL Mode

Application Information

1. Typical Application

This section describes a 2.1 Master and Slave application. The Master (U1 AXS2050w2JETQ EMC /P <</Lang (en-US)



3. Detailed Design Procedure

The AXS2050 devices are very flexible and easy-to-use Class D amplifiers; therefore, the design process is



4. Power Supply Recommendations

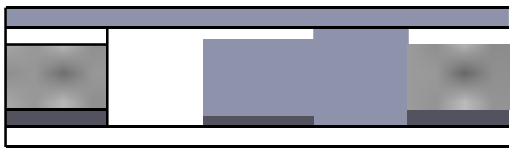
The AXS2050 device requires an external power supply, between 4.5 V and 26 V, for the analog circuitry (AVCC) and the power stage (PVCC) of the amplifier. Several on-chip regulators are included on the AXS2050 to generate the voltages necessary for the internal circuitry of the audio path. The voltage regulators which have been integrated are sized only to provide the current necessary to power the internal circuitry. The external pins are provided only as a connection point for off-chip bypass capacitors to filter the supply. Connecting external circuitry to these regulator outputs may result in reduced performance and damage to the device. The AVCC supply feeds internal LDO including GVDD. This LDO output are connected to external pins for filtering purposes, but should not be connected to external circuits. GVDD LDO output have been sized to provide current necessary for internal functions but not for

5. Layout Example



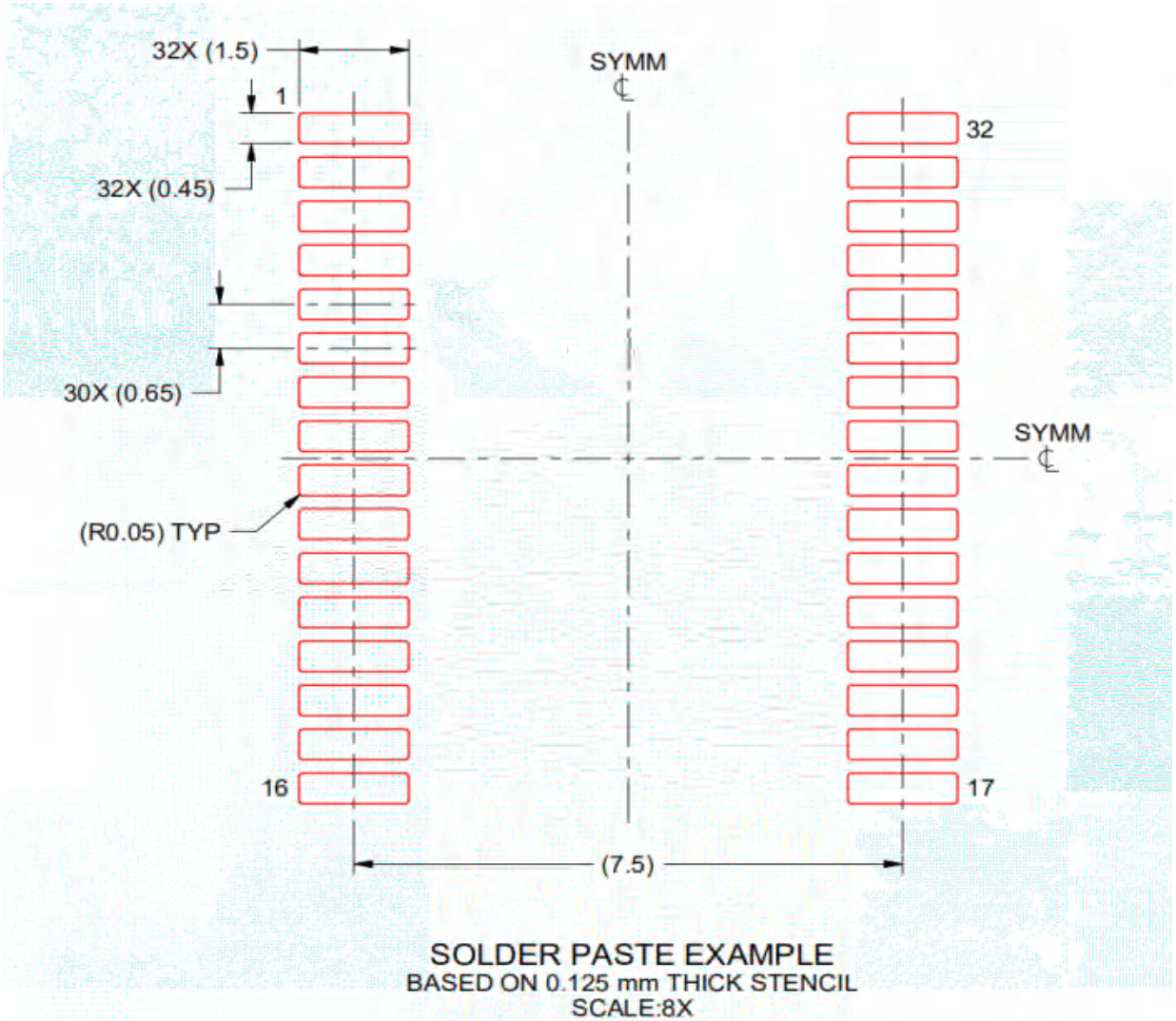
图33. Layout

6.



HTSSOP32





SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

