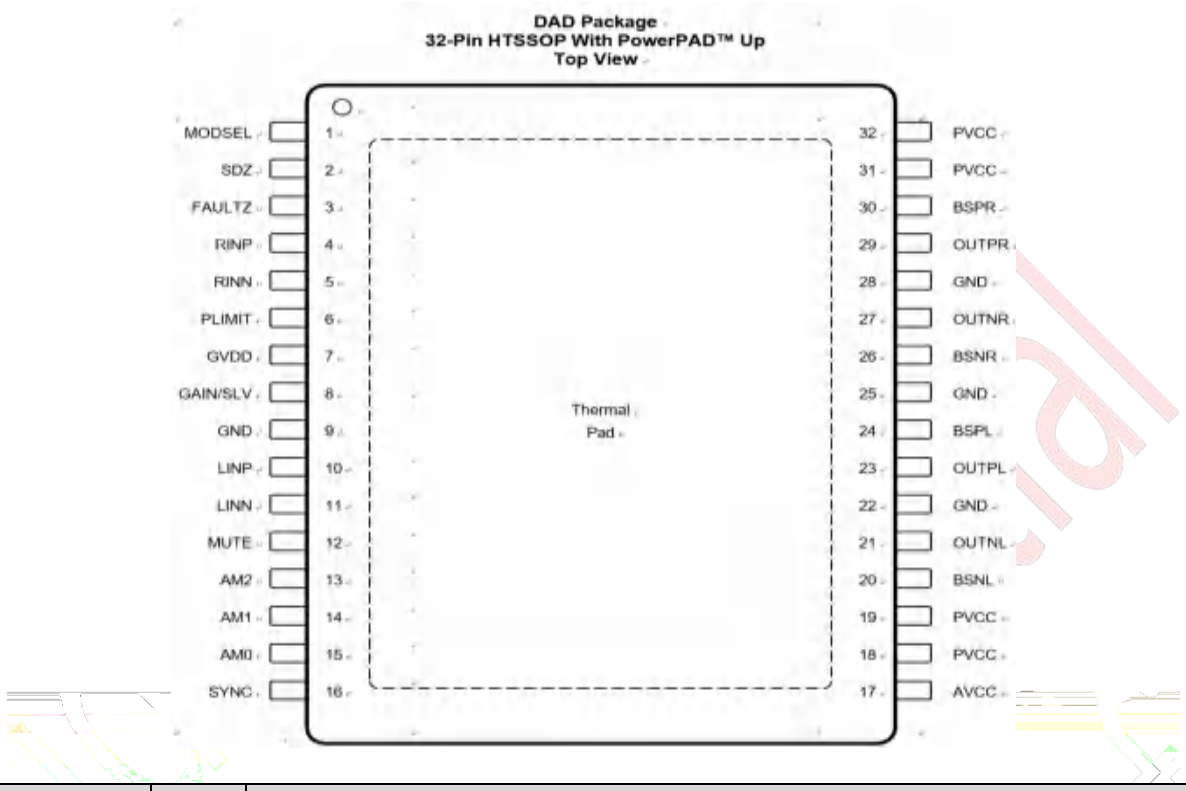
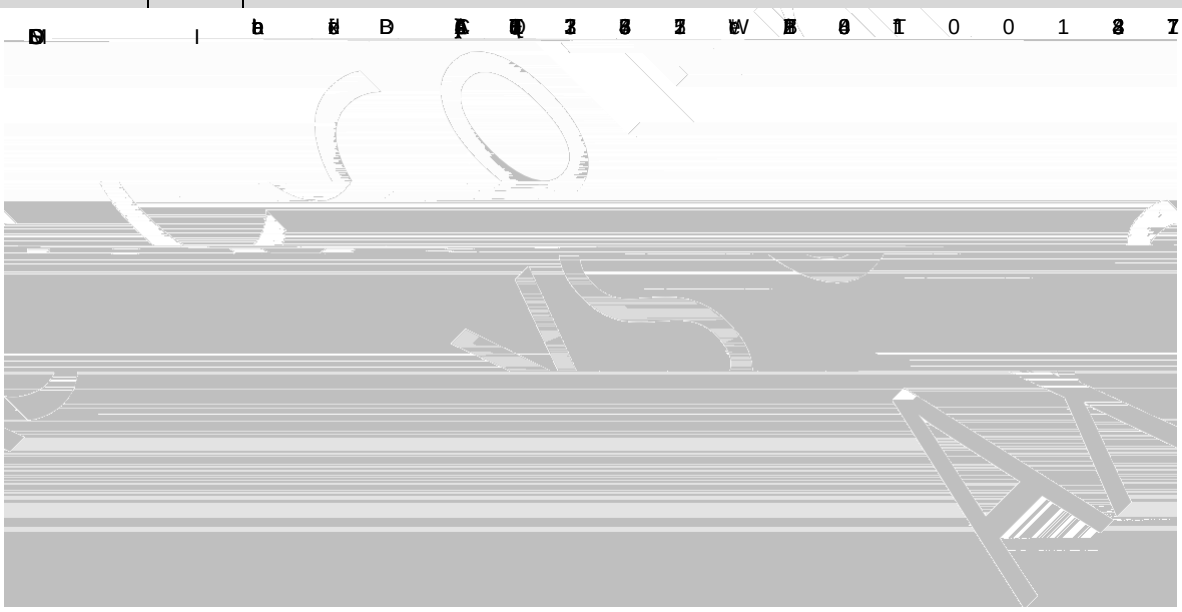
Description

Pin Configuration and Functions



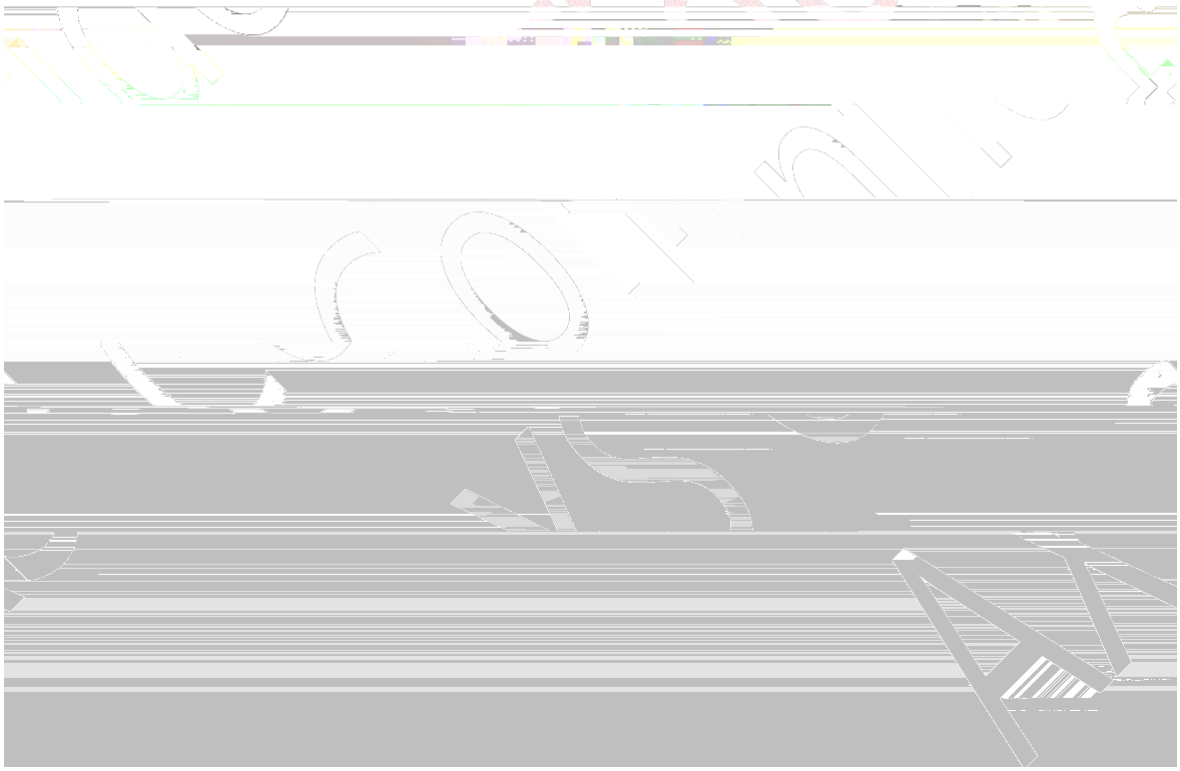
PIN		TYPE(1)	DESCRIPTION
NO.	NAME		
1	[illegible]	I	[illegible]



3. Recommended Operating Conditions

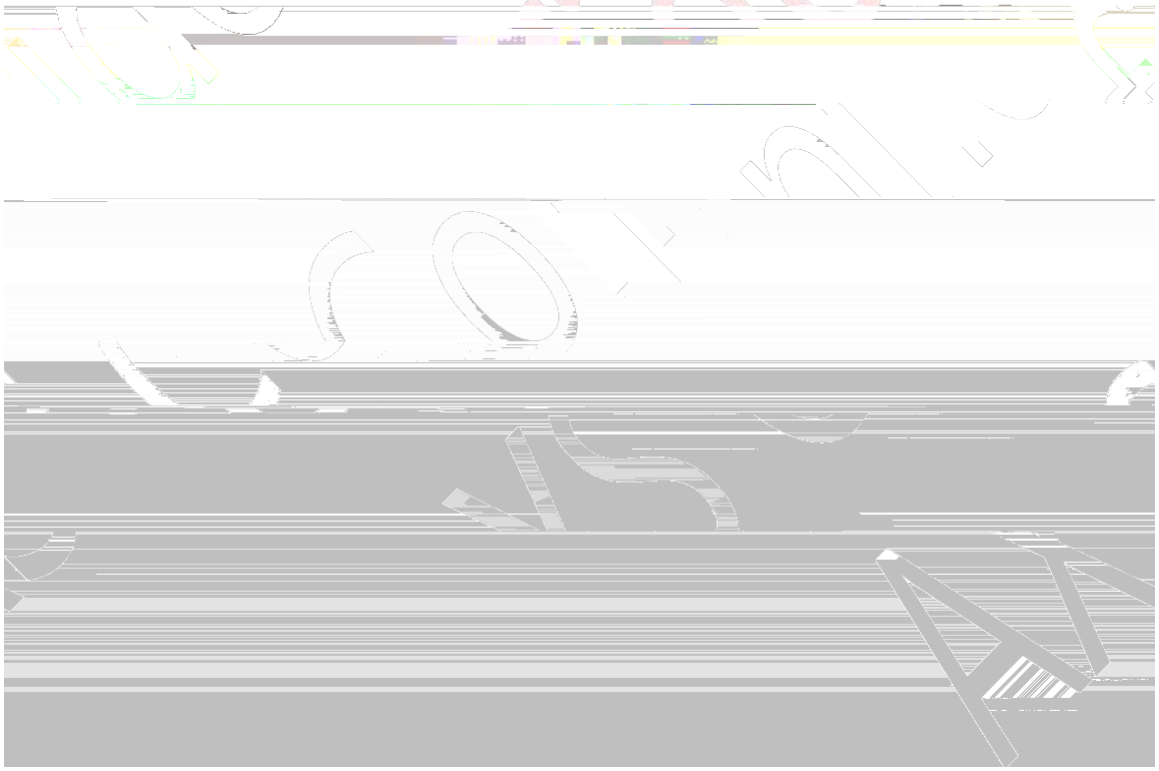
over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_C		5		12	V
V_H					



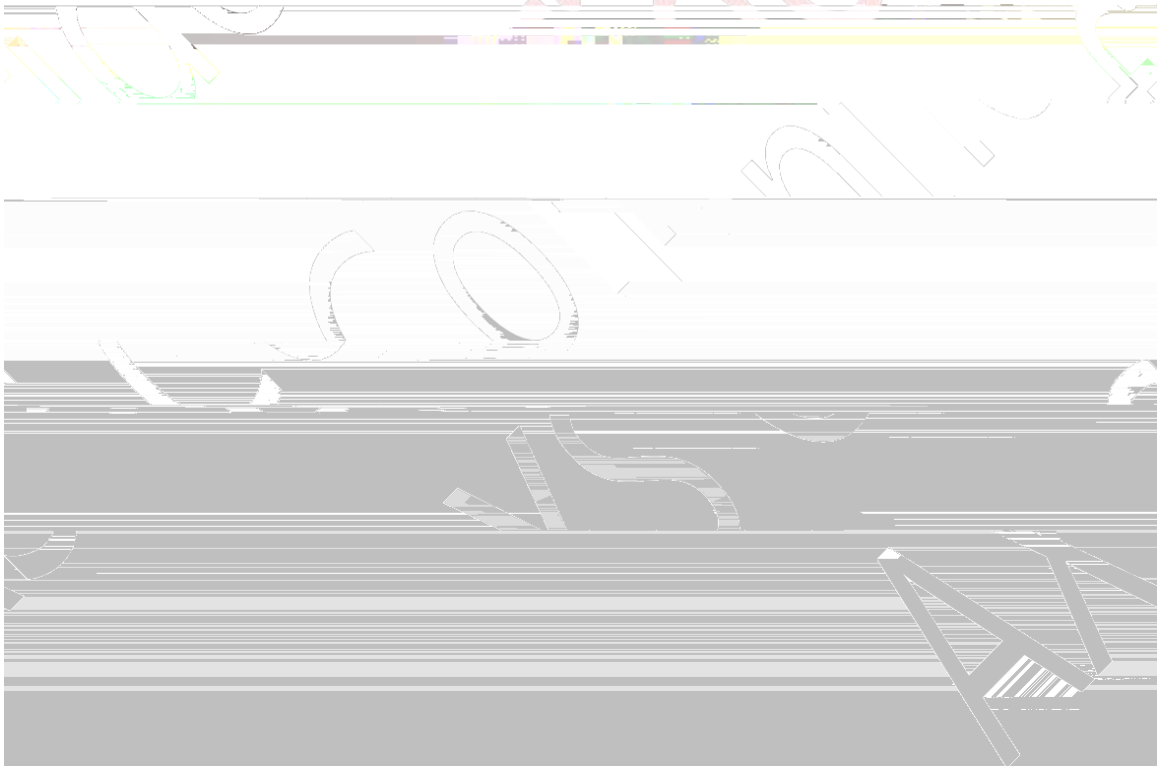
7. Typical Characteristics

f_S = 400kHz(unlessotherwisenoted)



Typical Characteristics (continued)

f_S = 400kHz(unlessotherwisenoted)



Detailed Description

1. Overview

2. Functional Block Diagram

3. Feature Description

3.1 Gain Setting and Master and Slave

The gain of the AXS2050 is set by the voltage applied to the GAIN/SLV pin. A resistor divider between GVDD and GND is used to set the voltage at the GAIN/SLV pin. The AXS2050 has 8 possible gain settings. The gain is set when the device is enabled or when recovering from a fault. Changing the gain during operation is not supported.

The AXS2050 can be configured as a master or slave in BTL mode. When configured as a master, the oscillator is active and the oscillator signal is available on the OSC_OUT pin. When configured as a slave, the oscillator is inactive and the oscillator signal is received on the OSC_OUT pin. Figure 1 shows the connection between the master and slave devices.

Table 1. Gain and Master/Slave

MASTER / SLAVE MODE	GAIN	R1 (to GND)(1)	R2 (to GVDD)(1)	INPUT IMPEDANCE

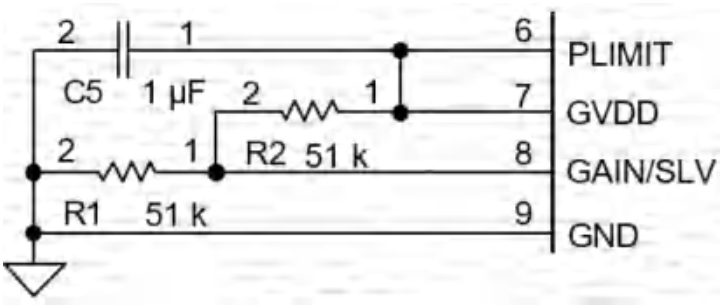


Table2. Recommended Input AC-Coupling Capacitors

GAIN	INPUT IMPEDANCE	INPUT CAPACITANCE	HIGH-PASS FILTER
0 B	6 k	5 F	2 H
0 B	2 k	3 F	9 H
3 B	2 k	6 F	3 H
6 B	3 k	0 F	2 H

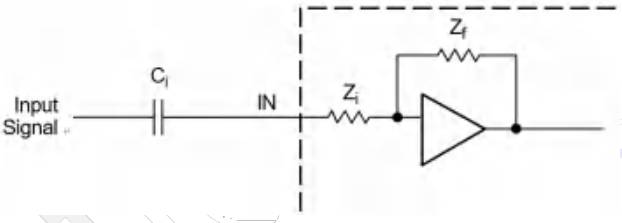
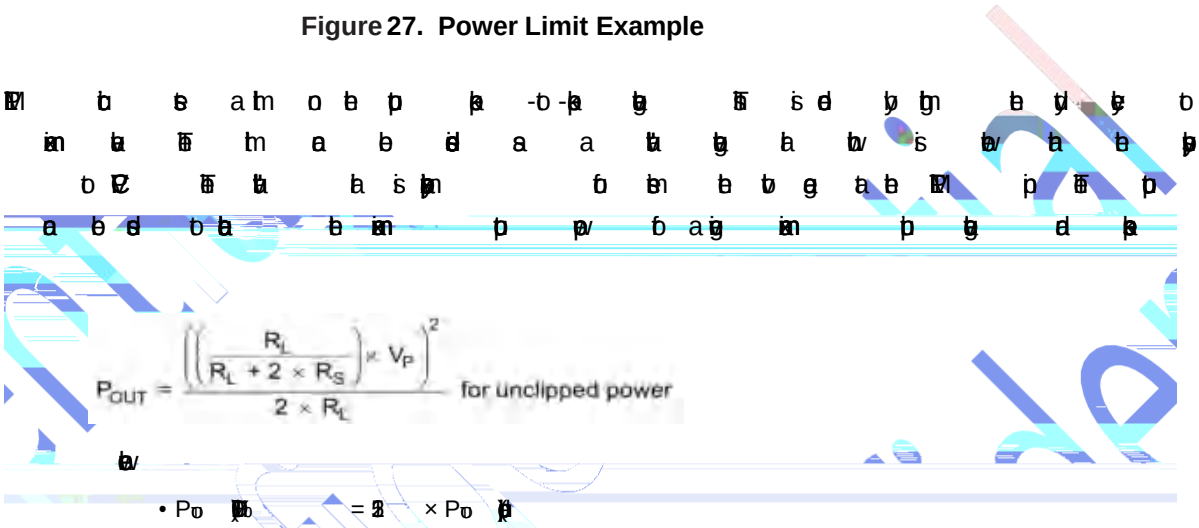


Figure 26. Input Impedance

3.3 Startup and Shutdown Operation

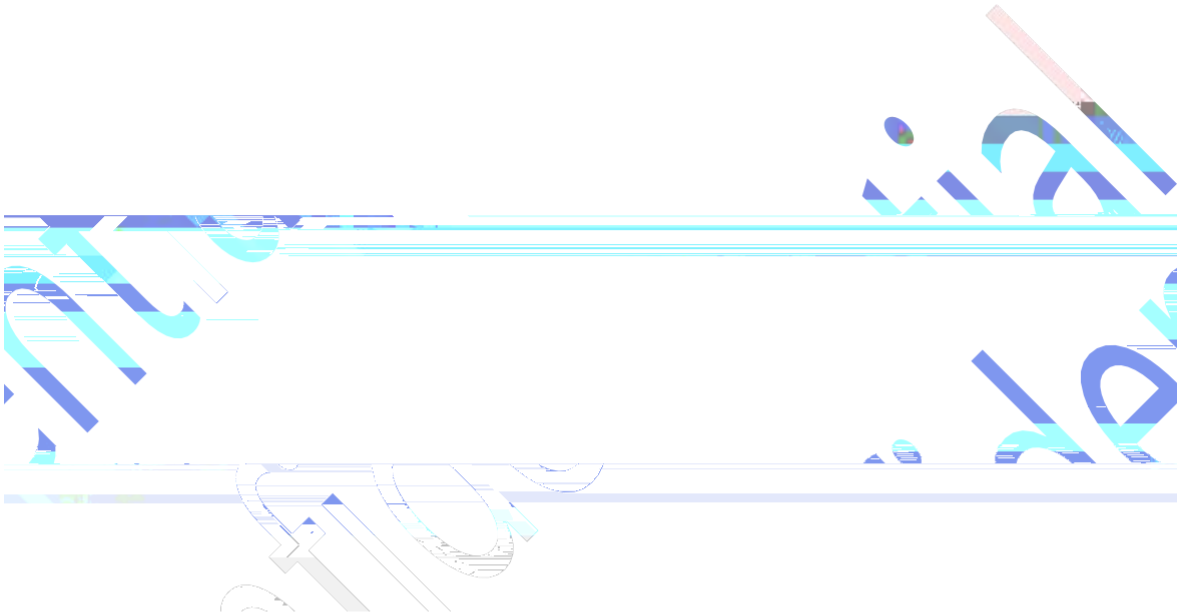
Figure 27. Power Limit Example



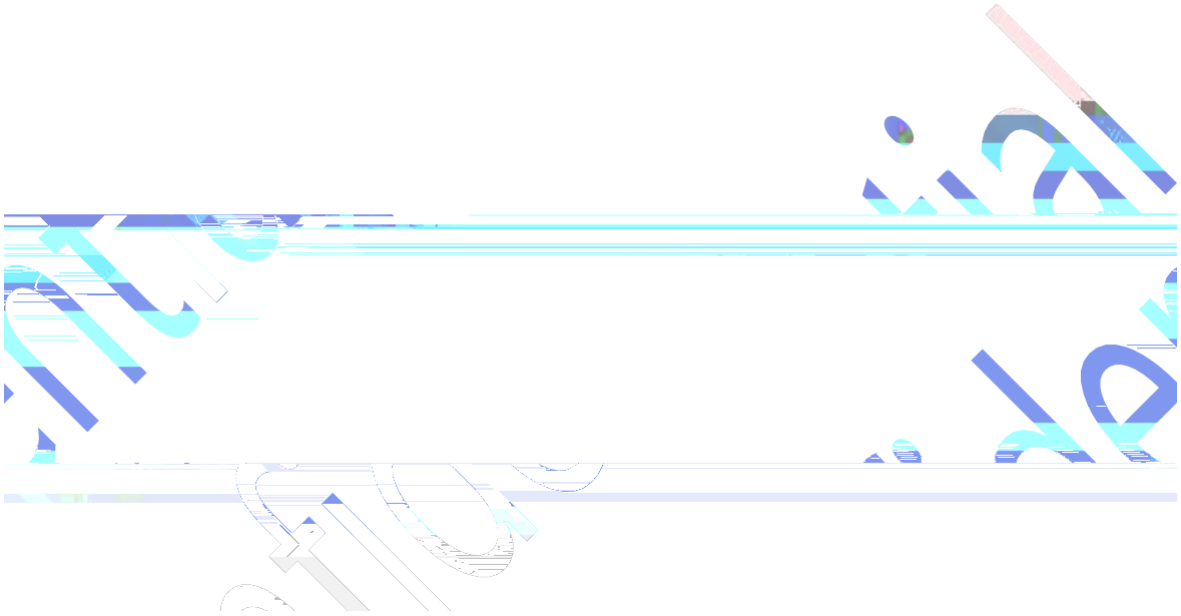
- Table 3. Power Limit Example

PVcc (V)	PLIMIT VOLTAGE (V)(1)	R to GND	R to GVDD	

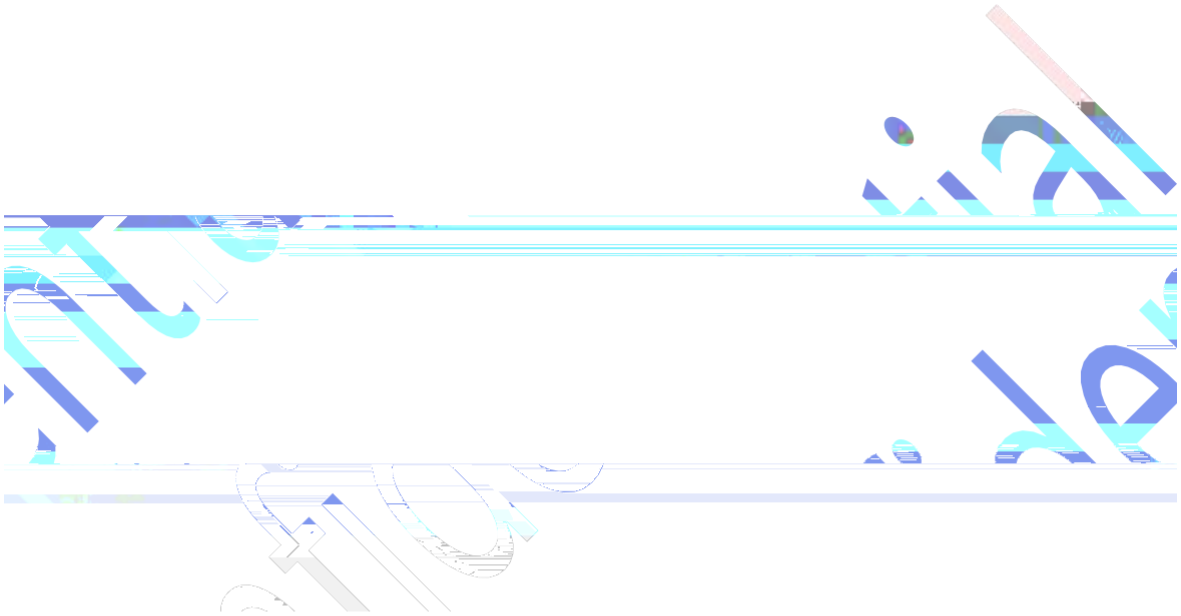
3.9 DC Detect Protection



4. Device Modulation Scheme







7. When to Use an Output Filter for EMI Suppression

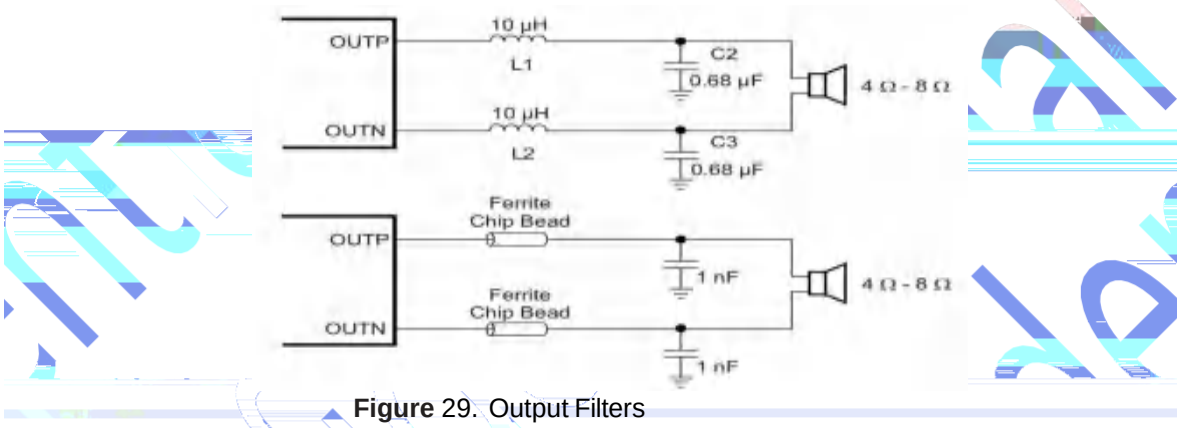


Figure 29. Output Filters

8. AM Avoidance EMI Reduction

Table 6. AM Frequencies

US	EUROPEAN	SWITCHING FREQUENCY (kHz)	AM2	AM1	AM0
AM FREQUENCY (kHz)	AM FREQUENCY (kHz)				
6 -2	6 -9	6	0	0	1
2 -1	9 -2	0 ǫ 0	0 0	1 0	0 0
1 -3	2 -3	6	0	0	1
3 -5	3 -8	0 ǫ 0	0 0	1 0	0 0
5 -0	8 -1	0 ǫ 0	0 0	1 0	0 1

9. Device Functional Modes

In the

9.1 Mono PBTL Mode

h om B eh be id a id p b -W l pv G p f om B
eh a a fv

- G N d N g b G fv pa s e id is s in a om B eh g pv p
- G B d N g f e p pa an d D d P g f e g pa an
- g p g is d b N d N

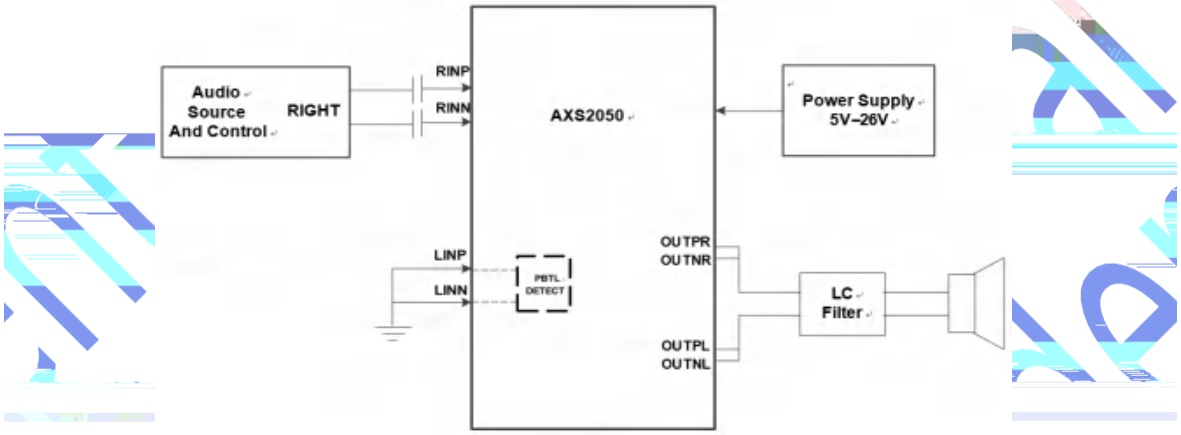


Figure 30. Mono PBTL Mode

9.2 Mono BTL

Mode (Single Channel Mode)

F A a e d in om B eh fv g e d pv o

eh

Application Information

1. Typical Application

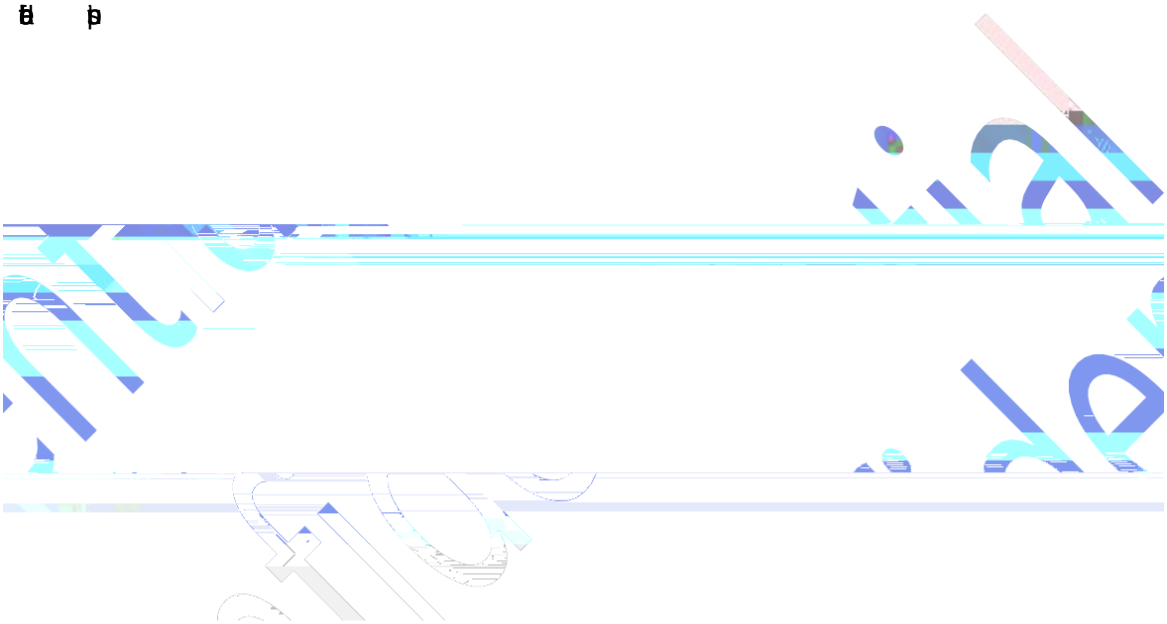


Figure 32. AXS2050 in a 2.1 Mode Application

2. Design Requirements

DESIGN PARAMETERS	EXAMPLE VALUE
	5 V to

3. Detailed Design Procedure

- [illegible]

3.1 Select the PWM Frequency

[illegible]

3.2 Select the Amplifier Gain and Master/Slave Mode

[illegible]

3.3 Select Input Capacitance

[illegible]

3.4 Select Decoupling Capacitors

[illegible]

3.5 Select Bootstrap Capacitors

[illegible]

6. Heat Sink Used on the EVM

The heat sink part number is ATS-TO220-21-C1-R0 or equivalent.

